IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate having an array region and a peripheral region formed adjacent to the array region;

a memory cell formed on the array region, and including a first gate insulator having a first thickness;

a high-voltage transistor circuit formed on the peripheral region, and including a second gate insulator having a second thickness greater than the first thickness; and

a dummy pattern formed adjacent to the high-voltage transistor circuit and including a third gate insulator, the third gate insulator having a thickness equal to the thickness of the second gate insulator and a height equal to the height of the second gate insulator.

2. (Currently Amended) A device according to claim 1, wherein the high-voltage transistor circuit includes a row decoder circuit ~~peripheral circuit is a guard ring, and arranged in a well region formed with the memory cell array~~.

3. (Currently Amended) A non-volatile semiconductor memory ~~device according to claim 1, wherein the peripheral circuit is a guard ring, and arranged between the memory cell array and the high-voltage transistor circuit~~ comprising:

a semiconductor substrate having an array region and a peripheral region formed adjacent to the array region;

a memory cell formed on the array region, and including a first gate insulator having a first thickness;

a high-voltage transistor circuit formed on the peripheral region, and including a second gate insulator having a second thickness greater than the first thickness; and

a guard ring formed between the memory cell and the high-voltage transistor circuit and including a third gate insulator, the third gate insulator having a thickness equal to the thickness of the second gate insulator and a height equal to the height of the second gate insulator.

4. (Currently Amended) A device according to claim 3, wherein the high-voltage transistor circuit includes a row decoder ~~the guard ring is arranged adjacent to the high-voltage transistor~~ circuit.

5. (Currently Amended) A non-volatile semiconductor memory device comprising: ~~according to claim 1, wherein the peripheral circuit is a dummy pattern, and arranged around the high-voltage transistor circuit~~.

a semiconductor substrate having an array region and a peripheral region formed adjacent to the array region;

a memory cell formed on the array region, and including a first gate insulator having a first thickness;

a high-voltage transistor circuit formed on the peripheral region, and including a second gate insulator having a second thickness greater than the first thickness;

a guard ring formed between the memory cell and the high-voltage transistor circuit, and including a third gate insulator; and

a dummy pattern formed adjacent to the high-voltage transistor circuit, and including a fourth gate insulator,

wherein a thickness of each of the third and fourth gate insulators is equal to the

thickness of the second gate insulator and a height of each of the third and fourth gate insulators is equal to the height of the second gate insulator.

6. (Currently Amended) A device according to claim 5, wherein the high-voltage transistor circuit includes ~~1, wherein the high-voltage transistor circuit constitutes~~ a row decoder circuit.

7. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

successively depositing a first gate insulator having a first thickness, a first gate electrode film and a first mask insulator on a semiconductor substrate;

leaving the first gate insulator, the first gate electrode film and the first mask insulator in only an array region;

separately forming the following gate insulators in a peripheral region excepting the array region, that is, forming a second gate insulator having a second thickness greater than the first thickness in a first region of a peripheral region, and forming a third gate insulator having a thickness the same as the first thickness in a second region of the peripheral region;

successively depositing a second gate electrode film and a second mask insulator thicker than the first mask insulator on each of the first mask insulator, the second gate insulator and the third gate insulator;

removing the second mask insulator and the second gate electrode film on the first mask insulator;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and first and second regions of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

8. (Withdrawn) A method according to claim 7, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.

9. (Withdrawn) A method according to claim 7, wherein the first region is formed with a row decoder circuit including a high-voltage transistor, and the second region is formed with a peripheral circuit including a guard ring and a dummy pattern.

10. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

successively depositing a first gate insulator having a first thickness, a first gate electrode film and a first mask insulator on a semiconductor substrate;

leaving the first gate insulator, the first gate electrode film and the first mask insulator in only an array region and a first peripheral region;

forming a second gate insulator having a second thickness greater than the first thickness in a second peripheral region excepting the array region and the first peripheral region;

successively depositing a second gate electrode film thinner than the first gate electrode film and a second mask insulator on each of the first mask insulator and the second gate insulator;

removing the second mask insulator and the second gate electrode film on the first mask insulator;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and first and second regions of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

11. (Withdrawn) A method according to claim 10, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.

12. (Withdrawn) A method according to claim 10, wherein the second mask insulator is formed to have approximately the same height as the first mask insulator.

13. (Withdrawn) A method according to claim 10, wherein the second peripheral region is formed with a row decoder circuit including a high-voltage transistor circuit.

14. (Withdrawn) A method according to claim 10, wherein the first peripheral region is formed with a peripheral circuit including a guard ring and a dummy pattern.

15. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

previously forming a recess in a first peripheral region on a semiconductor substrate;

forming a first gate insulator having a first thickness in the recess;

forming a second gate insulator having a second thickness less than the first thickness in an array region and a second peripheral region on the semiconductor substrate;

successively depositing first and second gate electrode films and first and second mask insulators on each of the first and second gate insulators;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and the first and second regions of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

16. (Withdrawn) A method according to claim 15, wherein the depth of the recess is substantially the same as the thickness of the first gate insulator.

17. (Withdrawn) A method according to claim 15, wherein the first and second gate electrode films and the first and second mask insulators are formed to have substantially the same thickness, respectively.

18. (Withdrawn) A method according to claim 15, wherein the first peripheral region is formed with a row decoder circuit including a high-voltage transistor circuit.

19. (Withdrawn) A method according to claim 15, wherein the second peripheral region is formed with a peripheral circuit including a guard ring and a dummy pattern.

20. (Withdrawn) A method according to claim 15, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.